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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/384,973	08/30/1999	HIDEKAZU TAKAHASHI	35.C13765	8552

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EXAMINER

HANNETT, JAMES M

ART UNIT	PAPER NUMBER
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2612

DATE MAILED: 04/10/2003

7

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/384,973

Applicant(s)

TAKAHASHI, HIDEKAZU

Examiner

James M Hannett

Art Unit

2612

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-12 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1012 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 30 August 1999 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on ____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 5.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). ____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other:

Specification

Drawings

1: Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

2: Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

3: The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: Solid State Image sensing apparatus which minimizes noise by setting the gains of the pixels sensor units different from the gains of the pixel memory units.

Claim Rejections - 35 USC § 102

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4: Claims 1-3, and 12 are rejected under 35 U.S.C. 102(b) as being anticipated by USPN 5,698,844 Shinohara et al.

Art Unit: 2612

5: As for Claim 1, Shinohara depicts in Figure 5 and on Column 7, Lines 55-67 and on Column 8, Lines 38-40 a photographic conversion apparatus comprising: a sensor unit including a plurality of pixels (sensor cells) each having at least photoelectric converting means (D) and first amplifying means (M_{13,15}) for amplifying a signal derived from the photoelectric converting means to output the amplified signal; and a memory unit (memory cell) including a plurality of memories each having at least storing means (Cs) for storing therein the signal derived from the sensor unit and second amplification means (M_{33,34}) for amplifying a signal derived from the storage means (Cs) to output an amplified signal wherein a gain of the first amplifying means (M_{13,15}) is made different from a gain of the second amplifying means (M_{33,34}), Column 5, Line 64. Shinohara teaches that the gain of the pixel sensor cell can be greater than 1. Shinohara further teaches that the gain of the memory cell unit is equal to -1. The first amplifying means is the amplifier in the sensor cell, and the second amplifying means is the amplifier in the memory cell.

6: In regards to Claim 2, Shinohara teaches that the first amplifying means (M_{13,15}) and the second amplifying means (M_{33,34}) are constituted by MOS transistors, Column 7, Lines 63-64 and Column 8, Lines 38-39.

7: As for Claim 3, Shinohara teaches in Figure 5 the first amplifying means and the second amplifying means are constituted by both amplifying MOS transistors and load MOS transistors. The amplifying transistor for the first amplifier is viewed as (M13) and the Load MOS for the first amplifier is viewed as (M14). As for the Second amplifying means the amplifying transistor is viewed as (M33) and the load transistor is viewed as (M34). Column 7, Lines 65-67 and

Art Unit: 2612

Column 8, Lines 41-43. These transistors are viewed as load transistors because they supply a predetermined voltage to the sensor cell and the memory cell respectively.

8: In regards to Claim 12, Shinohara teaches in Figure 5 that the photographic converting apparatus further comprising transferring means (Transfer Unit) for amplifying the signal derived from the sensor unit to transfer the amplified signal to the memory unit, Column 8, Lines 16-34.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

9: Claims 4-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over USPN 5,698,844 Shinohara et al in view of Official Notice.

10: In regards to Claim 4, Official notice is taken that it was commonly known in the art at the time the invention was made that the gain of a MOS amplifier was governed by the Channel length, Channel width, conductance, and gate oxide layer thickness of each of the MOS's in an amplifier. Therefore, it was commonly known in the art at the time the invention was made to change any of the parameters that effect the gain of an amplifier in order to obtain a desired gain for an amplifier circuit. As supported by USPN 6,163,215 Shibata et al Column 9, Lines 8-20. Shinohara et al teaches that the gains of the two amplifiers are different. In order to enable the two amplifiers to have different gains it was well known to one of ordinary skill in the art at the time the invention was made to vary the conductance of the load MOS transistor included in the

Art Unit: 2612

first amplifying mean is made different from a conductance of the load MOS transistor included in the second amplifying means. In order to vary the gains of the two amplifiers.

11: As for Claim 5, Official notice is taken that it was commonly know in the art at the time the invention was made to vary the gate length of a MOS in order to vary its gain. Therefore, Shinohara et al in view of Official Notice teaches that a gate length of the load MOS transistor included in the first amplifying means can be made different from a gate length of the load MOS transistor included in the second amplifying means. In order to vary the gains of the two amplifiers.

12: In regards to Claim 6, Official notice is taken that it was commonly know in the art at the time the invention was made to vary the gate width of a MOS in order to vary its gain. Therefore, Shinohara et al in view of Official Notice teaches that a gate width of the load MOS transistor included in the first amplifying means can be made different from a gate length of the load MOS transistor included in the second amplifying means. In order to vary the gains of the two amplifiers.

13: As for Claim 7, Official notice is taken that it was commonly know in the art at the time the invention was made to vary the oxide layer thickness of a MOS in order to vary its gain. Therefore, Shinohara et al in view of Official Notice teaches that a gate oxide layer thickness of the load MOS transistor included in the first amplifying means can be made different from a gate oxide layer thickness of the load MOS transistor included in the second amplifying means. In order to vary the gains of the two amplifiers.

14: In regards to Claim 8, Official notice is taken that it was commonly known in the art at the time the invention was made that the gain of a MOS amplifier was governed by the Channel

Art Unit: 2612

length, Channel width, conductance, and gate oxide layer thickness of each of the MOS's in an amplifier. Therefore, it was commonly know in the art at the time the invention was made to change any of the parameters that effect the gain of an amplifier in order to obtain a desired gain for an amplifier circuit. As supported by USPN 6,163,215 Shibata et al Column 9, Lines 8-20. Shinohara et al teaches that the gains of the two amplifiers are different. In order to enable the two amplifiers to have different gains it was well know to one of ordinary skill in the art at the time the invention was made to vary the conductance of the amplifying MOS transistor included in the first amplifying means is made different from a conductance of the amplifying MOS transistor included in the second amplifying means. In order to vary the gains of the two amplifiers.

15: As for Claim 9, Official notice is taken that it was commonly know in the art at the time the invention was made to vary the gate length of a MOS in order to vary its gain. Therefore, Shinohara et al in view of Official Notice teaches that a gate length of the amplifying MOS transistor included in the first amplifying means is made different from a gate length of the amplifying MOS transistor included in the second amplifying means. In order to vary the gains of the two amplifiers.

16: In regards to Claim 10, Official notice is taken that it was commonly know in the art at the time the invention was made to vary the gate width of a MOS in order to vary its gain. Therefore, Shinohara et al in view of Official Notice teaches that a gate width of the amplifying MOS transistor included in the first amplifying means is made different from a gate width of the amplifying MOS transistor included in the second amplifying means. In order to vary the gains of the two amplifiers.

Art Unit: 2612

17: As for Claim 11, Official notice is taken that it was commonly know in the art at the time the invention was made to vary the oxide layer thickness of a MOS in order to vary its gain. Therefore, Shinohara et al in view of Official Notice teaches that a gate oxide layer thickness of the amplifying MOS transistor included in the first amplifying means can be made different from a gate oxide layer thickness of the amplifying MOS transistor included in the second amplifying means. In order to vary the gains of the two amplifiers.

Conclusion

18: The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. USPN 6,163,215 Shibata et al discusses the equations by which the gain of a MOS amplifier is governed; USPN 5,717,458 Yonemoto teaches a Solid state image sensor that has charge detection circuits, amplifiers, and charge storage circuits.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James M Hannett whose telephone number is 703-305-7880. The examiner can normally be reached on 8:00 am to 5:00 pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wendy Garber can be reached on 703-305-4929. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9314 for regular communications and 703-842-9314 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to customer service whose telephone number is 703-308-6789.


Application/Control Number: 09/384,973

Page 8

Art Unit: 2612

James Hannett
Examiner
Art Unit 2612

JMH
April 2, 2003



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